7.5 A 10b Driver IC for a Spatial Optical Modulator for Full HDTV Applications

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The spatial optical modulator (SOM) is a kind of diffractive spatial light-modulator (SLM), like a micro-mirror device (DMD) [1], a grating light valve (GLV) [2], or a grating electromechanical system (GEMS) [3]. Figure 7.5.1 shows the optical modulation scheme and the single-pixel ribbon structure of the SOM. This SOM utilizes piezoelectric actuation of an individual grating light micro-mirror in which we can control it's displacement of the micro-mirror from the bottom reflector [4]. A SOM-based laser rear projection display system with full high-definition (HD) format, 60Hz frame rate, and 8b per color was successfully developed and demonstrated [4]. For future applications, however, a display system with color depth greater than 8b and enhanced image quality with more than 120 frames per second is inevitable. Therefore, we developed the 10b SOM driver IC with 120Hz frame rate for full HDTV applications.

Although the structure of the SOM driver IC is very similar to that of a TFT-LCD driver IC, there are some problems to overcome because of the unique features in its driving method and conditions, and the physical characteristics of the SOM device. First, the line time for full HDTV using the SOM device is only 4μs due to the frame rate of 120Hz and vertical scanning method. Moreover, the programming time for the output buffer must be less than 2.4μs in order to provide enough diffraction time during the line time. A constant slew is required during the programming time because of the response characteristic of the SOM. Second, the dynamic range of the unity-gain amplifier output is only from 2.4 to 6V. This means that the voltage difference between adjacent gray levels is so small that the unity-gain operational amplifier must have accurate output voltage levels. In the worst case, the allowable error voltage for the unity-gain operational amplifier is less than 1.2mV for the 10b linear DAC. Third, a compact 10b DAC is one of the critical requirements in designing this driver IC. The area of a conventional resistor-string DAC doubles for every 1 bit increase of the image data. So a 10b DAC based on a decoder and a resistor string has 4 times more area than an 8b DAC. Since even the 8b DAC takes 60 to 70% of the total area of the 8b data driver, the 10b DAC of this type is almost impractical [5].

To drive a capacitive load during the programming time with a constant slew rate, it is necessary that the DAC structure perform digital-to-analog (DA) conversion and drive the capacitive load simultaneously. We can't use a DAC that divides the row line time into DA conversion time, output buffer driving time, and diffraction time like an R-C DAC does [5]. An R-R DAC [6] is a candidate, but it needs such large channel resistors that an area efficient driver IC cannot be achieved. As a result, we use a new type of 10b DAC consisting of both a 7b resistor-string DAC and an operational amplifier that includes a 3b DAC. The block diagram is shown in Figure 7.5.2. The 7b resistor string DAC selects two voltages that correspond to adjacent gray levels that bracket the value to be converted. The 3b decoder generates 8 outputs by combining these two voltages. These 8 outputs correspond to the least significant 3b of the digital word. The positive input stage of the output buffer is split into 8 branches and the 8 output signals from the 3b decoder are supplied to these branches. This structure allows the circuit to perform DA conversion and to drive a capacitive load at the same time. The area of the new 10b DAC is only 25% larger than that of the 7b resistor-string DAC.

Figure 7.5.3 shows a schematic diagram that explains the operating principle of the DAC that is embedded into an operational amplifier. Compared to a conventional operational amplifier, this operational amplifier has a positive input stage that contains two split transistors, M1 and M2. Assume that V_L is supplied to the gate of M2, V_H, which is equal to $V_L + \Delta V$, is supplied to the gate of M3, and the gate of M4 is connected to the output, V_F. Also assume that W/L is the same for both M2 and M3 and that (W/L) of M4 is twice as large. The current relationships for M2, M3 and M4 can be expressed as:

$$V_F - V_{N2} - V_{th} = \sqrt{\left(V_L - V_{N2} - V_{th} + \frac{\Delta V}{2}\right)^2 + \frac{1}{4}(\Delta V)^2} \quad (1)$$

where V_{N2} is the voltage at node N2. Equation (1) can be expressed using a power series as:

$$V_F = V_L + \frac{\Delta V}{2} + \alpha \quad (2)$$

where α is a higher-order term of the power series. Equation (2) shows that a negative input voltage has a value between V_L and V_H when the input stage is composed of only NMOS transistors. On the contrary, if the input stage is composed of PMOS transistors and $\beta(C_{OX} \cdot W/L)$ is the same value for the NMOS and PMOS transistors, the output voltage will be represented as:

$$V_F = V_L + \frac{\Delta V}{2} - \alpha. \quad (3)$$

From (2) and (3) we notice that α can be removed when the input stage is composed of PMOS and NMOS transistors that share their gate nodes. Consequently, the output voltage has a value between V_L and V_H without any DA conversion errors.

Figure 7.5.4 shows the schematic diagram of the 3b DAC embedded into the output buffer and it shows the practically implemented circuit using the concept of Figure 7.5.3. Figure 7.5.5 shows the simulation results of the output buffer shown in Figure 7.5.4. These results verify that the output buffer performs a 3b DA conversion when digital data changes from '000' to '111' where V_{DD} is 15V, V_{SS} is 0V, V_L is 10.459V and V_H is 10.506V. Figure 7.5.5 also shows that the output voltages are spaced 6mV apart and the errors of the output voltages are less than 1mV.

A 546-channel 10b SOM driver IC is fabricated in a 0.35μm 3.3V/18V CMOS process technology. The driver IC consists of a mini-LVDS input stage, a digital control block, a 7b resistor-string DAC, and the unity-gain amplifier with a 3b linear DAC. We verified the performance of the output buffer by measuring its output voltages. Figure 7.5.6 shows the measured output voltages when the digital inputs to all channels are the 528th gray level. In Figure 7.5.6, the difference between the maximum voltage and the minimum voltage, which is the offset error of the output buffer, is less than 1mV. Figure 7.5.6 also shows the maximum difference voltages when the digital inputs to all channels change from 0 to full scale. With the same digital inputs, the voltage differences of the output buffers are all less than 1.3mV. Figure 7.5.7 shows a micrograph of the fabricated driver IC. Its area is 21,700μm×3,000μm. The low-voltage operating blocks, such as the digital circuits and mini-LVDS input stages, consume 10.9mA at 3.3V and the high-voltage analog circuits consume 65mA at 15V.

References:

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[6] Y.-C. Sung, et al., "10bit Source Driver with Resistor-Resistor-String Digital to Analog Converter," *SID'05 Dig.*, Vol. 36, pp. 1099-1101, May, 2005.

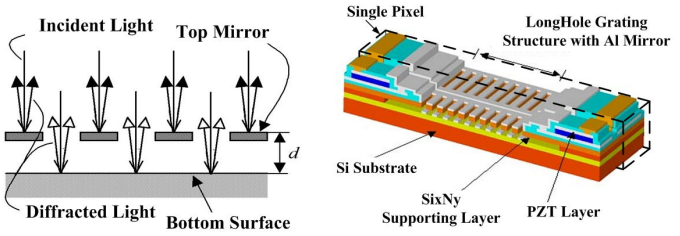

Figure 7.5.1: The optical modulation scheme and single-pixel ribbon structure of the SOM.

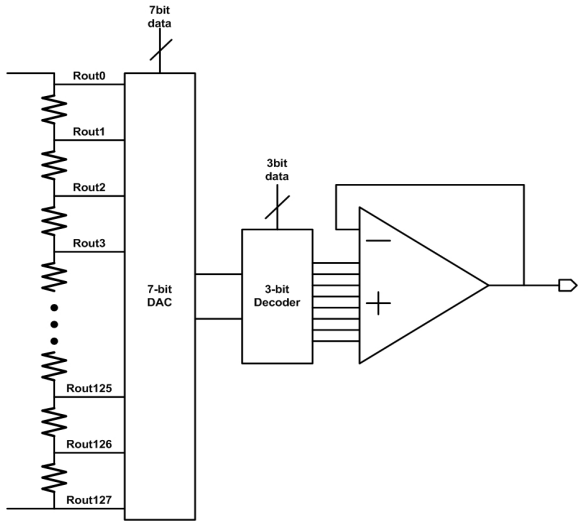

Figure 7.5.2: Block diagram of a 10b DAC with a 7b resistor-string DAC and an operational amplifier that includes a 3b DAC.

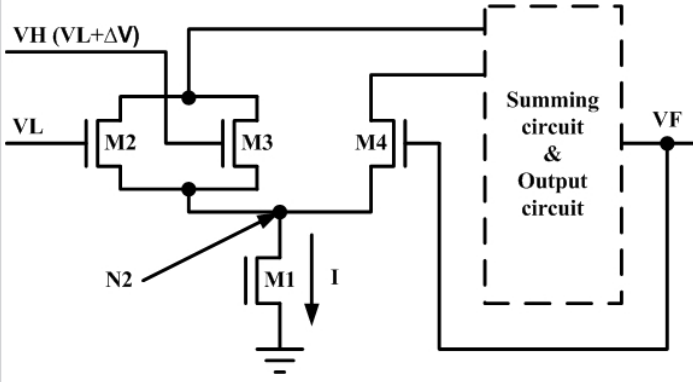

Figure 7.5.3: Schematic diagram of the DAC that is embedded into an operational amplifier.

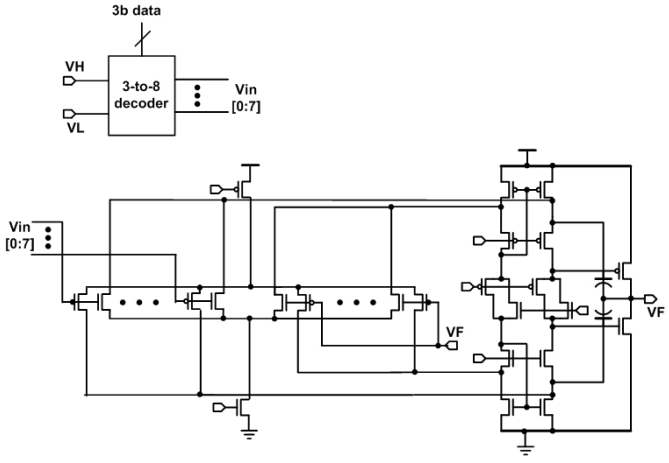

Figure 7.5.4: Schematic diagram of the 3b DAC that is embedded into an operational amplifier.

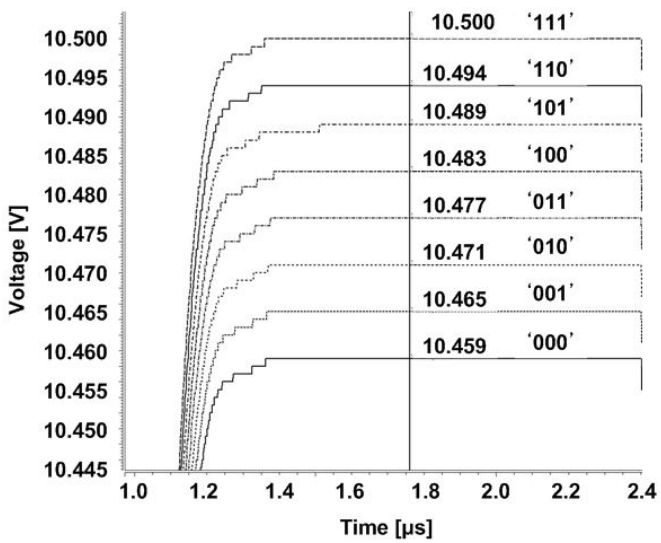

Figure 7.5.5: Simulation results of the output buffer.

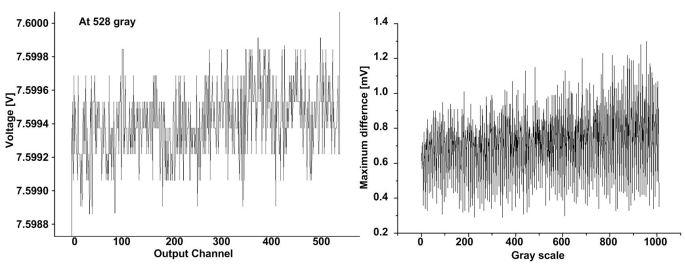

Figure 7.5.6: Measured results for channel uniformity.

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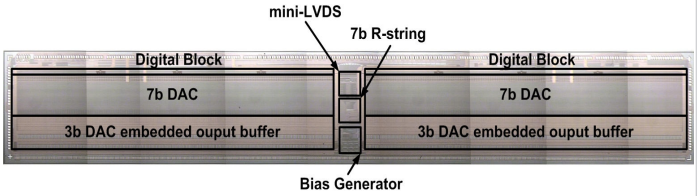

Figure 7.5.7: Micrograph of the fabricated driver IC.

